In the claims:

Please cancel claim 1 and amend claim 2 as follows:

1. (cancelled)

2. (currently amended) ~~The differential clock-presence detector of claim 1 further comprising:~~

A differential clock-presence detector comprising:

a true differential clock line and a complement differential clock line alternately driven to opposite states when a differential clock is present and pulsing;

an output capacitor coupled to an output node;

a first differential transistor, having a gate receiving the true differential clock line, for drawing a first discharge current;

a first mirror transistor, coupled to the first differential transistor, for generating a first mirror current in response to a bias voltage applied to a gate of the first mirror transistor;

a second differential transistor, having a gate receiving the complement differential clock line, for drawing a second discharge current;

a second mirror transistor, coupled to the second differential transistor, for generating a second mirror current in response to the bias voltage applied to a gate of the second mirror transistor;

wherein pulsing of the differential clock draws the first and second currents from the output capacitor to drive the output node to a clock-present state; and

a leaker for driving a leakage current to the output node, the leakage current being less than the first discharge current,

wherein loss of the differential clock causes the leakage current to drive the output node to a clock-loss state,

whereby presence of the differential clock is detected.

3. (original) The differential clock-presence detector of claim 2 further comprising:

a first diode, coupled between the first differential transistor and the output capacitor; and

a second diode, coupled between the second differential transistor and the output capacitor.

4. (original) The differential clock-presence detector of claim 3 further comprising:
a current sink, coupled to the first and second differential transistors, for sinking a tail current from the first and second differential transistors.

5. (original) The differential clock-presence detector of claim 4 wherein the first and second differential transistors are n-channel transistors having sources connected together and to the current sink;
wherein the first and second mirror transistors are p-channel transistors having sources connected to a power supply;
wherein drains of the first mirror transistor and the first differential transistor are connected together and to the first diode;
wherein drains of the second mirror transistor and the second differential transistor are connected together and to the second diode.

6. (original) The differential clock-presence detector of claim 5 wherein the first diode is a n-channel transistor having a gate and a drain connected together and to the output node;
wherein the second diode is a n-channel transistor having a gate and a drain connected together and to the output node.

7. (original) The differential clock-presence detector of claim 2 further comprising:
a buffer, coupled to the output node, for buffering the output node to generate a clock-loss signal.

8. (original) The differential clock-presence detector of claim 7 wherein the output capacitor is connected between the output node and a power supply;

wherein the output capacitor and the output node are discharged low when the differential clock is pulsing, but rises high by the leakage current when the differential clock stops pulsing.

9. (original) The differential clock-presence detector of claim 2 further comprising:

a first resistor, coupled between the true differential clock line and a common-mode node;

a second resistor, coupled between the complement differential clock line and the common-mode node;

a bias transistor that receives the common-mode node at a gate to generate a bias current in response to a common-mode voltage of the common-mode node; and

a bias mirror transistor, coupled to the bias transistor and passing the bias current, for setting the bias voltage,

whereby the bias voltage is set by the common-mode voltage.

10. (original) The differential clock-presence detector of claim 9 further comprising:

a common-mode capacitor coupled to the common-mode node,

whereby the common-mode voltage is averaged by the common-mode capacitor.

11. (original) A differential clock detector comprising:

a first differential clock input and a second differential clock input that together form a differential clock input;

tail current means for drawing a tail current from a tail node;

integrating capacitor means for storing charge on an integrating node;

first differential transistor means, coupled between a first node and the tail node, for generating a first current in response to the first differential clock input;

first current source means, coupled to the first node, for sourcing current to the first differential transistor means;

first diode means, coupled between the first node and the integrating node, for drawing the first current from the integrating capacitor means when the differential clock input is pulsing;

second differential transistor means, coupled between a second node and the tail node, for generating a second current in response to the second differential clock input;

second current source means, coupled to the second node, for sourcing current to the second differential transistor means; and

second diode means, coupled between the second node and the integrating node, for drawing the second current from the integrating capacitor means when the differential clock input is pulsing,

whereby first and second currents are integrated by the integrating capacitor means to detect presence of pulsing of the differential clock input.

12. (original) The differential clock detector of claim 11 further comprising:

buffer means for buffering the integrating node to generate a clock-loss signal; and

leaker means, coupled to the integrating node, for providing a leakage current to the integrating capacitor means, the leakage current being offset by the first and second currents when the differential clock input is pulsing, but the leakage current causing the clock-loss signal to be driven to an active state when the differential clock input is not pulsing,

whereby the clock-loss signal is activated to indicate loss of pulsing of the differential clock input.

13. (original) The differential clock detector of claim 12 wherein the first current is drawn from the integrating capacitor means when the first differential clock input is high, while second current is drawn from the integrating capacitor means when the second differential clock input is high,

whereby first and second currents are alternately drawn from the integrating capacitor means as the differential clock input is pulsing.

14. (original) The differential clock detector of claim 13 further comprising:

common-mode means, coupled between the first and second differential clock inputs, for generating a common-mode voltage; and

bias-generator means, receiving the common-mode voltage, for generating a bias voltage to the first and second current source means to control currents generated by the first and second current source means,

whereby sourced currents are controlled by the common-mode voltage.

15. (original) The differential clock detector of claim 14 wherein the first differential transistor means and the second differential transistor means are n-channel transistors, and wherein the integrating capacitor means is a capacitor between the integrating node and a power supply, and the first current source means and the second current source means comprise p-channel transistors, or

the first differential transistor means and the second differential transistor means are p-channel transistors, and the integrating capacitor means is a capacitor between the integrating node and a ground, and the first current source means and the second current source means comprise n-channel transistors.

16. (original) A differential clock detect circuit comprising:

differential clock inputs that include a first differential clock line and a second differential clock line;

an output capacitor on an output node;

a first differential transistor with a gate that receives the first differential clock line, a drain coupled to a first node, and a source coupled to a source node;

a first current source transistor having a drain coupled to the first node and a gate driven by a bias node;

a first diode coupled between the first node and the output node, the first diode preventing backward current flow from the first current source transistor to the output node;

a second differential transistor with a gate that receives the second differential clock line, a drain coupled to a second node, and a source coupled to the source node;

a second current source transistor having a drain coupled to the second node and a gate driven by a bias node;

a second diode coupled between the second node and the output node, the second diode preventing backward current flow from the second current source transistor to the output node; and

a buffer, receiving the output node, for driving a clock-loss signal that indicates when the differential clock inputs are not pulsing,

whereby loss of differential clock pulsing is detected.

17. (original) The differential clock detect circuit of claim 16 wherein the first and second differential transistors are n-channel transistors, and the first and second current source transistors are p-channel transistors, or the first and second differential transistors are p-channel transistors, and the first and second current source transistors are n-channel transistors.

18. (original) The differential clock detect circuit of claim 17 further comprising:

a first resistor between the first differential clock line and a common node;

a second resistor between the second differential clock line and the common node;

a common-node capacitor on the common node;

a bias transistor receiving the common node at a gate, and having a drain connected to the bias node; and

a bias mirror transistor having a gate and a drain connected together and to the bias node, whereby bias to the first and second current source transistors is generated from the common node between the first and second differential clock lines.

19. (original) The differential clock detect circuit of claim 18 further comprising:

a leaker transistor having a drain connected to the output node, and a gate connected to a fixed voltage, the leaker transistor being a p-channel transistor having a source connected to a power supply when the first differential transistor is an n-channel transistor, but an n-channel transistor with a source connected to a ground when the first differential transistor is a p-channel transistor.

20. (original) The differential clock detect circuit of claim 19 further comprising:

a current sink transistor coupled between the source node and a ground.